WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an insulating film provided on a support substrate;

a first semiconductor layer provided on the insulating film;

a first memory cell constituting a part of a memory cell in an SRAM, having a first gate electrode of a first conductivity type on a gate insulating film on the first semiconductor layer and first source/drain diffusion layers of a second conductivity type opposite to the first conductivity type which sandwich a region under the first gate electrode in the first semiconductor layer, and fulfilling an expression such as the thickness of the first semiconductor layer $\leqq$ one-third of a length of the first gate electrode in its channel length direction;

a second semiconductor layer provided on the insulating film; and

a first peripheral transistor constituting a part of a peripheral circuit, having a third gate electrode on a gate insulating film on the second semiconductor layer and third source/drain diffusion layers which sandwich a region under the third gate electrode in the second semiconductor layer, and fulfilling an expression such as the thickness of the second semiconductor layer > one-third of a length of the

third gate electrode in its channel length direction.

2. The device according to claim 1, wherein the first and third gate electrodes consist essentially of Si_XGe_{1-X} ($0 \leqq X \leqq 1$).

3. The device according to claim 1, further comprising a second memory cell transistor which constitutes a part of the memory cell in the SRAM, has a second gate electrode of the second conductivity type on a gate insulating film on the first semiconductor layer and second source/drain diffusion layers of the first conductivity type sandwiching a region under the second gate electrode in the first semiconductor layer, and fulfills an expression such as the thickness of the first semiconductor layer $\leqq$ one-third of a length of the second gate electrode in its channel length direction.

4. The device according to claim 3, wherein the third source/drain diffusion layer and the third gate electrode are of the same conductivity type.

5. The device according to claim 4, further comprising a second peripheral transistor which constitutes a part of the peripheral circuit, has a fourth gate electrode on a gate insulating film on the second semiconductor layer and fourth source/drain diffusion layers sandwiching a region under the fourth gate electrode in the second semiconductor layer, and fulfills an expression such as the thickness of the

second semiconductor layer > one-third of a length of the fourth gate electrode in its channel length direction.

6. The device according to claim 5, wherein the fourth source/drain diffusion layers and the fourth gate electrode are of the same conductivity type.

7. The device according to claim 5, wherein the first, second, third, and fourth gate electrodes consist essentially of Si_XGe_{1-X} ($0 \leqq X \leqq 1$).

8. The device according to claim 1, wherein 90% or more of the volume of the first gate electrode consists of silicide.

9. The device according to claim 8, wherein the third gate electrode has silicide on only a part of its upper part.

10. The device according to claim 9, wherein the first gate electrode has a volume equal to 80% or less of the volume of the third gate electrode.

11. The device according to claim 8, further comprising a sidewall insulating film provided on the sidewall of the first gate electrode excluding its upper part.

12. The device according to claim 8, further comprising:

a first sidewall insulating film provided on the sidewall of the third gate electrode; and

a second sidewall insulating film provided on

the sidewall of the first gate electrode and having an upper end lower than the upper end of the first sidewall insulating film.

13. A semiconductor device comprising:

a semiconductor substrate;

an insulating film provided on the semiconductor substrate;

a semiconductor layer provided on the semiconductor substrate;

a first memory cell constituting a part of a memory cell in an SRAM, having a first gate electrode of a first conductivity type on a gate insulating film on the first semiconductor layer and first source/drain diffusion layers of a second conductivity type opposite to the first conductivity type which sandwich a region under the first gate electrode in the semiconductor layer, and fulfilling an expression such as the thickness of the semiconductor layer $\leqq$ one-third of a length of the first gate electrode in its channel length direction;

a first peripheral transistor constituting a part of a peripheral circuit, having a third gate electrode on a gate insulating film on the semiconductor substrate and third source/drain diffusion layers which sandwich a region under the third gate electrode in the semiconductor substrate.

14. The device according to claim 13, wherein the

first and third gate electrodes consist essentially made of Si_XGe_{1-X} ($0 \leqq X \leqq 1$).

15. The device according to claim 13, further comprising a second memory cell transistor which constitutes a part of the memory cell in the SRAM, has a second gate electrode of the second conductivity type on a gate insulating film on the semiconductor layer and second source/drain diffusion layers of the first conductivity type which sandwich a region under the second gate electrode in the semiconductor layer, and fulfills an expression such as the thickness of the semiconductor layer $\leqq$ one-third of a length of the second gate electrode in its channel length direction.

16. The device according to claim 15, wherein the third source/drain diffusion layers and the third gate electrode are of the same conductivity type.

17. The device according to claim 16, further comprising a second peripheral transistor which constitutes a part of the peripheral circuit, has a fourth gate electrode on a gate insulating film on the semiconductor substrate and fourth source/drain diffusion layers which sandwich a region under the fourth gate electrode in the semiconductor substrate.

18. The device according to claim 17, wherein the fourth source/drain diffusion layers and the fourth gate electrode are of the same conductivity type.

19. The device according to claim 17, wherein

the first, second, third, and fourth gate electrodes consist essentially of Si_XGe_{1-X} ($0 \leqq X \leqq 1$).

20. The device according to claim 13, wherein 90% or more of the volume of the first gate electrode consists of silicide.

21. The device according to claim 20, wherein the third gate electrode has silicide on only a part of its upper part.

22. The device according to claim 21, wherein the first gate electrode has a volume equal to 80% or less of the volume of the third gate electrode.

23. The device according to claim 20, further comprising a sidewall insulating film provided on the sidewall of the first gate electrode excluding its upper part.

24. The device according to claim 20, further comprising:

a first sidewall insulating film provided on the sidewall of the third gate electrode; and

a second sidewall insulating film provided on the sidewall of the first gate electrode and having an upper end lower than the upper end of the first sidewall insulating film.

25. A semiconductor device comprising:

an insulating film provided on a support substrate;

a first semiconductor layer provided on the

insulating film;

a first memory cell constituting a part of a memory cell in an SRAM, having a first gate electrode consisting essentially of a metal material on a gate insulating film on the first semiconductor layer and first source/drain diffusion layers which sandwich a region under the first gate electrode in the first semiconductor layer, and fulfilling an expression such as the thickness of the first semiconductor layer $\leqq$ one-third of a length of the first gate electrode in its channel length direction;

a second semiconductor layer provided on the insulating film; and

a first peripheral transistor constituting a part of a peripheral circuit, having a third gate electrode on a gate insulating film on the second semiconductor layer and third source/drain diffusion layers which sandwich a region under the third gate electrode in the second semiconductor layer, and fulfilling an expression such as the thickness of the second semiconductor layer > one-third of a length of the third gate electrode in its channel length direction.

26. The device according to claim 25, wherein the first gate electrode consists essentially made of a material selected from a group consisting of tungsten, titanium, molybdenum, nickel, cobalt, platinum, and an alloy of these metals.

27. A semiconductor device comprising:

a semiconductor substrate;

an insulating film provided on the semiconductor substrate;

a semiconductor layer provided on the semiconductor substrate;

a first memory cell constituting a part of a memory cell in an SRAM, having a first gate electrode consisting essentially of a metal material on a gate insulating film on the first semiconductor layer and first source/drain diffusion layers which sandwich a region under the first gate electrode in the semiconductor layer, and fulfilling an expression such as the thickness of the semiconductor layer $\leqq$ one-third of a length of the first gate electrode in its channel length direction;

a first peripheral transistor constituting a part of a peripheral circuit, having a third gate electrode on a gate insulating film on the semiconductor substrate and third source/drain diffusion layers which sandwich a region under the third gate electrode in the semiconductor substrate.

28. The device according to claim 27, wherein the first gate electrode consists essentially of a material selected from a group consisting of tungsten, titanium, molybdenum, nickel, cobalt, platinum, and an alloy of these metals.

29. A semiconductor device comprising:

an insulating film provide on a support substrate;

a first semiconductor layer provided on the insulating film;

a first memory cell constituting a part of a memory cell in an SRAM, having a gate electrode on a gate insulating film on a first side of the first semiconductor layer, on a second side opposite to the first side, and on the top in contact with the first and second sides, having first source/drain diffusion layers which sandwich a region enclosed by the first gate electrode in the first semiconductor layer;

a second semiconductor layer provided on the insulating film; and

a first peripheral transistor constituting a part of a peripheral circuit, having a third gate electrode on a gate insulating film on the second semiconductor layer and third source/drain diffusion layers which sandwich a region under the third gate electrode in the second semiconductor layer, and fulfilling an expression such as the thickness of the second semiconductor layer > one-third of a length of the third gate electrode in its channel length direction.

30. A semiconductor device manufacturing method comprising:

forming a first semiconductor layer with a first thickness on an insulating film on a support substrate

in a first region where a memory cell transistor constituting a part of a memory cell in an SRAM is to be formed;

forming a second semiconductor layer with a second thickness greater than the first thickness on the insulating film in a third region where a peripheral transistor constituting a part of a peripheral circuit is to be formed;

implanting an impurity of a first conductivity type into the second semiconductor layer in the third region;

forming a conductive film above the first and second semiconductor layers;

implanting an impurity of a second conductivity type opposite to the first conductivity type into the conductive film in the third region;

implanting an impurity of the first conductivity type into the conductive film in the first region;

forming from the conductive film a first gate electrode which fulfills an expression such as the first thickness $\leqq$ one-third of a length of the first gate electrode in its channel length direction in the first region and a third gate electrode which fulfills an expression such as the second thickness > one-third of a length of the third gate electrode in its channel length direction from the conductive film in the third region; and

forming a first and third source/drain diffusion layers of the second conductivity type in the first and second semiconductor layers in the vicinity of the first and third gate electrodes, respectively.

31. The method according to claim 30, wherein forming the first semiconductor layer and the second semiconductor layer includes

forming a semiconductor layer with the second thickness on the insulating film,

oxidizing the upper part of the semiconductor layer in the first region, and

removing the oxidized part of the semiconductor layer.

32. The method according to claim 30, wherein forming the first semiconductor layer and the second semiconductor layer includes

forming a semiconductor layer with the first thickness on the insulating film, and

growing the semiconductor layer in the second region to the second thickness.

33. The method according to claim 30, further comprising:

implanting an impurity of the second conductivity type into the conductive film in a second region where a memory cell transistor constituting a part of the memory cell in the SRAM;

forming from the conductive film a second gate

electrode which fulfills an expression such as the first thickness ≦ one-third of a length of the second gate electrode in its channel length direction) in the second region; and

forming a second source/drain diffusion layer of the first conductivity type in the first semiconductor layer in the vicinity of the second gate electrode.

34. The method according to claim 33, further comprising:

implanting an impurity of the second conductivity type into the second semiconductor layer in a fourth region where a peripheral transistor constituting the peripheral circuit;

forming a fourth gate electrode which fulfills an expression such as the second thickness > one-third of a length of the second gate electrode in its channel length direction in the fourth region; and

forming a fourth source/drain diffusion layer of the first conductivity type in the second semiconductor layer in the vicinity of the fourth gate electrode.

35. The method according to claim 30, further comprising

turning 90% or more of the first gate electrode into silicide.

36. A semiconductor device manufacturing method comprising:

forming a first semiconductor layer with a first

thickness on an insulating film on a support substrate in a first region where a memory cell transistor constituting a part of a memory cell in an SRAM is to be formed;

forming a second semiconductor layer with a second thickness greater than the first thickness on the insulating film in a third region where a peripheral transistor constituting a part of a peripheral circuit is to be formed;

forming, on the second semiconductor layer in the third region, the peripheral transistor which has a third gate electrode provided on a gate insulating film on the second semiconductor layer and third source/drain diffusion layers that sandwich a region under the third gate electrode in the second semiconductor layer and which fulfills an expression such as the thickness of the second semiconductor layer > one-third of a length of the third gate electrode in its channel length direction;

forming a metal film consisting essentially of tungsten, titanium, molybdenum, nickel, cobalt, platinum, or an alloy of these metals above the first semiconductor layer in the first region;

forming from the metal film a first gate electrode which fulfills an expression such as the first thickness $\leqq$ one-third of a length of the first gate electrode in its channel length direction in the first

region; and

forming first source/drain diffusion layers in the first semiconductor layer in the vicinity of the first gate electrode.